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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEWIS, MONICA	
ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,917	KIM ET AL.	
	Examiner	Art Unit	
	MONICA LEWIS	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-20,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-20,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the request for continued examination filed February 19, 2008.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/19/08 has been entered.

Drawings

3. The drawings are objected to because of the following: a) each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either

"Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14, 16-18 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Hirler et al. (U.S. Patent No. 6,147,381) and Uenishi et al. (U.S. Patent No. 5,151,762).

In regards to claim 14, Applicant's Prior Art ("APA") discloses the following:

a) a semiconductor substrate (102) forming a collector region (For Example: See Figure 1A);

b) a drift region (106) of a first conductivity type extending over the semiconductor substrate (For Example: See Figure 1A);

c) first well region (108) of a second conductivity extending from an upper surface of the drift region into and terminating within the drift region, the first well being coupled to an emitter terminal (For Example: See Figure 2A);

d) a planar channel region (A) in an upper portion of the first well region (For Example: See Figure 1A); and

e) impurity region (210) of the first conductivity type (For Example: See Figure 2A).

In regards to claim 14, APA fails to disclose the following:

a) a second well region being in a floating state.

However, Hirler et al. ("Hirler") discloses a semiconductor device that has a second well region floating (15) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include a second well region floating as disclosed in Hirler because it aids in ensuring that the breakdown voltage is not reduced (For Example: See Abstract).

Additionally, since APA and Hirler are both from the same field of endeavor, the purpose disclosed by Hirler would have been recognized in the pertinent art of APA.

b) a second well region of a second conductivity extending from an upper surface of the drift region into and terminating within the drift region, the planar channel region and the second well region being separated by an impurity region, where the first well region and the second well region have a substantially same depth in the drift region.

However, Uenishi et al. ("Uenishi") discloses a semiconductor device that has a second well region (705) of a second conductivity extending from an upper surface of the drift region (703) into and terminating within the drift region, the planar channel region (708) and the second well region being separated by an impurity region, where the first well region and the second well region have a substantially same depth in the drift region (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include a second well region of a second conductivity extending from an upper surface of the drift region into and terminating within the drift region, the planar channel region and the second well region being separated by an impurity region, where the first well region and the second well region have a substantially

same depth in the drift region as disclosed in Uenishi because it aids in providing high breakdown voltage (For Example: See Column 6 Lines 9-16).

Additionally, since APA and Uenishi are both from the same field of endeavor, the purpose disclosed by Uenishi would have been recognized in the pertinent art of APA.

Finally, it would have been a matter of obvious design choice to have the first well region and the second well region have a substantially same depth in the drift region, since such a modification would have involved a mere change in the sizes of the components. A change in size is generally recognized as being with the level of ordinary skill in the art. See In re Rose, 105 USPQ 237 (CCPA 1955).

In regards to claim 16, APA discloses the following:

a) the impurity region has an impurity concentration higher than that of the drift region (For Example: See Figure 2A).

In regards to claim 17, APA discloses the following:

a) an emitter region (110) of the first conductivity type formed in an upper portion of the first well region, the emitter region being coupled to the emitter terminal (For Example: See Figure 2A); and

b) a gate terminal extending over but being insulated from the planar channel region (For Example: See Figure 2A).

In regards to claim 18, APA discloses the following:

a) a buffer layer (104) between the semiconductor substrate and the drift region and having the same conductivity type as the drift region, the buffer layer having a higher impurity concentration than the impurity region (For Example: See Figure 2A).

In regards to claim 33, APA fails to disclose the following:

a) the impurity region abuts the first well region and the second well region.

However, Uenishi discloses a semiconductor device that has an impurity region that abuts the first well region and the second well region (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include an impurity region that abuts the first well region and the second well region as disclosed in Uenishi because it aids in providing high breakdown voltage (For Example: See Column 6 Lines 9-16).

Additionally, since APA and Uenishi are both from the same field of endeavor, the purpose disclosed by Uenishi would have been recognized in the pertinent art of APA.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Hirler et al. (U.S. Patent No. 6,147,381), Uenishi et al. (U.S. Patent No. 5,151,762), Li (U.S. Patent No. 5,793,064) and Nishiura et al. (U.S. Patent No. 4,987,098).

In regards to claim 15, APA fails to disclose the following:

a) each of the first and second well regions form a separate pn junction with the impurity region such that when the separate pn junctions are reverse biased a boundary of depletion region in the drift region is substantially flat.

However, Li discloses a semiconductor device that has first and second well regions (180 and 190) form separate pn junctions with the impurity region (177) such that when the separate pn junctions are reverse biased a boundary of depletion region (For Example: See Column 8 Lines 32-54). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include first and second well regions and an impurity region therebetween configured such that when the separate pn junctions are reverse biased a boundary of depletion region as disclosed in Li because it aids in blocking high voltage (For Example: See Column 8 Lines 32-54).

Additionally, since APA and Li are both from the same field of endeavor, the purpose disclosed by Li would have been recognized in the pertinent art of APA.

b) the depletion region is substantially flat.

However, Nishiura et al. ("Nishiura") discloses a semiconductor device that has a depletion region (22) that is substantially flat (For Example: See Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include a depletion region that is substantially flat as disclosed in Nishiura because it aids in overcoming problems with hole current (For Example: See Column 2 Lines 3-22).

Additionally, since APA and Nishiura are both from the same field of endeavor, the purpose disclosed by Nishiura would have been recognized in the pertinent art of APA.

7. Claims 19 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Hirler et al. (U.S. Patent No. 6,147,381), Uenishi et al. (U.S. Patent No. 5,151,762) and Uenishi (U.S. Patent No. 5,008,720).

In regards to claim 19, APA fails to disclose the following:

a) a distance between the well regions is in a range of 3 um to 6 um.

However, Uenishi discloses a semiconductor device that has a distance (B) between the well regions that are in a range of 3 um to 6 um (For Example: See Table 1B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include well regions that are in a range of 3 um to 6 um as disclosed in Uenishi because it aids in providing a device that can not be easily broken down due to overload (For Example: See Column 3 Lines 30-33).

Additionally, since APA and Uenishi are both from the same field of endeavor, the purpose disclosed by Uenishi would have been recognized in the pertinent art of APA.

Finally, the applicant has not established the critical nature of a distance between the first well region and the second well region is in a range of 3 um to 6 um. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

In regards to claim 32, APA fails to disclose the following:

a) a distance between the well regions is in a range of 4 um to 5 um.

However, Uenishi discloses a semiconductor device that has a distance (B) between the well regions that are in a range of 4 um to 5 um (For Example: See Table 1B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include well regions that are in a range of 4 um to 5 um as disclosed in Uenishi because it aids in providing a device that can not be easily broken down due to overload (For Example: See Column 3 Lines 30-33).

Additionally, since APA and Uenishi are both from the same field of endeavor, the purpose disclosed by Uenishi would have been recognized in the pertinent art of APA.

Finally, the applicant has not established the critical nature of a distance between the first well region and the second well region is in a range of 4 um to 5 um. "The law is replete with

cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Hirler et al. (U.S. Patent No. 6,147,381), Uenishi et al. (U.S. Patent No. 5,151,762) and Matsudai et al. (European Patent Application No. EP 1193767).

In regards to claim 20, APA fails to disclose the following:

a) the thickness of the drift region is in a range of 40 um to 120 um.

However, Matsudai et al. ("Matsudai") discloses a semiconductor device that has a drift region (13) with a thickness in a range of 40 um to 120 um (For Example: See Paragraph 31). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of APA to include a drift region (13) with a thickness in a range of 40 um to 120 um as disclosed in Matsudai because it aids in controlling the breakdown voltage (For Example: See Paragraph 28).

Additionally, since APA and Matsudai are both from the same field of endeavor, the purpose disclosed by Matsudai would have been recognized in the pertinent art of APA.

Finally, the applicant has not established the critical nature of the thickness of the drift region is in a range of 40 um to 120 um. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims.

. . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

Response to Arguments

9. Applicant's arguments filed 2/19/08 have been fully considered but they are not persuasive. First, Applicant argued that "Hirler requires that p+ floating regions 15 have a depth distinctly greater than that of shielding zone 13…Hirler fails to teach two well regions that have substantially the same depth." However, Hirler is not being utilized to teach a first well region and a second well region that have substantially the same depth in the drift region. Hirler is being utilized to disclose the use of a well in a floating state.

Finally, Applicant argued that "both well regions 705 in Fig. 8 of Uenishi are connected to cathode terminal K and thus neither well region 705 is in a floating state...thus combining the teachings of Hirler with AAP or Uenishi results in formation of two p-type regions that are not of substantially the same depth." However, Uenishi is not being utilized to disclose the use of a well in a floating state. Hirler is being utilized to teach a first well region and a second well region that have substantially the same depth in the drift region (For Example: See Figure 8).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MONICA LEWIS whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

/Monica Lewis/
Primary Examiner, Art Unit 2822

April 4, 2008